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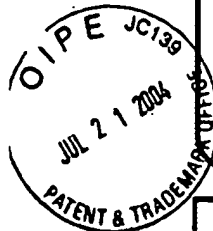
Substitute for form 1449A/PTO

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Sheet 1 of 3

Application Number	10/718,662
Filing Date	November 24, 2003
First Named Inventor	Edwin C. Kan
Group Art Unit	2827 2827
Examiner Name	
Attorney Docket Number	CRF D-2768/Kan



U.S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

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**Examiner
Signature**

Date
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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/718,662
		Filing Date	November 24, 2003
		First Named Inventor	Edwin Kan
		Group Art Unit	2818 2827
		Examiner Name	
Sheet 2	of 3	Attorney Docket Number	CRF D-2768/Kan

7/21/04

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.†	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T‡
DL	1	J.R. Tucker, "Schottky barrier MOSFETs for Silicon nanoelectronics," Advanced Workshop on Frontiers in Electronics, WOFE'97 Proceedings, pp. 97-100, 1997.	
	2	C. Wang, J.P. Snyder and J.R. Tucker, "Sub-40 nm PtSi Schottky source/drain metal-oxide-semiconductor field-effect transistors," Appl. Phys. Lett, vol. 74, pp1174-6, 1999.	
	3	V. Narayanan, Z. Liu, Y.M.N. Shen, M. Kim and E.C. Kan, "Reduction of metal-semiconductor contact resistance by embedded nanocrystals," IEDM Tech. Dig., pp. 87-90, 2000.	
	4	E.C. Kan and Z. Liu, "Directed self-assembly process for nano-electronic devices and interconnect," Superlattices and Microstructures, vol. 27, pp. 473-9, 2000.	
	5	Z. Liu, M. Kim, V. Narayanan, and E.C. Kan, "Process and device characteristics of self-assembled metal nano-crystal EEPROM," Superlattices and Microstructures, vol. 28, pp. 393-9, 2000.	
	6	Z. Suo and Z. Zhang, Epitaxial films stabilized by long range forces," Phys. Rev. B, vol. 58, pp. 5116-20, 1998.	
	7	D.A. Bonnell, Y. Liang, M. Wagner, D. Carroll and M. Buhle, "Effect of size dependent interface properties on stability of metal clusters on ceramic substrates," Acta Mater., vol. 46, pp. 2263-70, 1998.	
	8	Z. Liu, V. Narayanan, M. Kim, G. Pei and E.C. Kan, "Low programming voltages and long retention time in metal nanocrystal EEPROM devices," 59th DRC Tech. Dig., pp. 79-80, 2001.	
	9	H.C. Lin, E.C. Kan, T. Yamanaka & C.R. Helms, "Modeling and characterization of Si/SiO2 interface roughness," VLSI Tech. Symp., Kyoto, Japan, June 1997.	
	10	J. Kedzierski, P. Xuan, E.H. Anderson, J. Bokor, T.J. King and C. Hu, "Complementary silicide source/drain thin-body MOSFETs for the 20nm gate length regime," IEDM Tech. Dig., pp. 57-60, 2000.	
DL	11	J. Kedzierski, P. Xuan, V. Subramanian, E.H. Anderson, J. Bokor, T.J. King and C. Hu, "A 20-nm gate-length ultra-thin body p-MOSFET with silicide source/drain," Si Nanoelectronics Workshop, VLSI Tech. Symp., pp. 13-15, Honolulu, Hawaii, June 2000	

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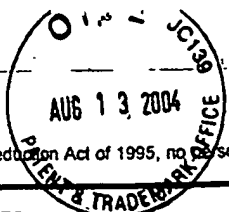
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known	
		Application Number	10/718,662
		Filing Date	November 24, 2003
		First Named Inventor	Edwin C. Kan
		Art Unit	2827
		Examiner Name	
Sheet 1 of 3	Attorney Docket Number	CRF D-2768D/Kan	

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
DL	1	"The Evolution of Dram Cell Technology," B. El-Kareh, G.B. Bromner; Solid State Technology, May 1997, Vol. 40, Issue 5	
	2	"Fast and Long Retention-Time Nano-Crystal Memory," H.I. Hanafi, S. Tiwari, I. Khan; IEEE Transactions on Electron Devices, Vol. 43, No. 9, September 1996	
	3	"Charge-Trap Memory Device Fabricated by Oxidation of Si _{1-x} Ge _x ," Y-C King, T-J King, C. Hu; IEEE Transactions on Electron Devices, Vol. 48, No. 4, April 2001	
	4	"A Long-Refresh Dynamic/Quasi-Nonvolatile Memory Device with 2-nm Tunneling Oxide," Y-C King, T-J King, C. Hu; IEEE Electron Device Letters, Vol. 20, No. 8, August 1999	
	5	"NR0M: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell," B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, D. Finzi; IEEE Electron Device Letters, Vol. 21, No. 11, November 2000	
	6	"A Low Voltage SONOS Nonvolatile Semiconductor Memory Technology," M.H. White, Y. Yang, A. Purwar, M.L. French; IEEE Transactions on Components, Packaging, and Manuf. Tech.-Part A, Vol. 20, No. 2, June 1997	
	7	"High-Endurance Ultra-Thin Tunnel Oxide in MONOS Device Structure for Dynamic Memory Application," H.C. Wann, C. Hu; IEEE Electron Device Letters, Vol. 16, No. 11, November 1995	
	8	"Programming Characteristics of P-Channel Si Nano-Crystal Memory," K. Han, I. Kim, H. Shin; IEEE Electron Device Letters, Vol. 21, No. 6, June 2000	
DL	9	"A Novel, aerosol-nanocrystal floating-gate device for non-volatile memory applications," J. DeBlauwe, M. Ostraat, M.L. Green, G. Weber, T. Sorsch, A Kerber, F. Klemens, et al.; 2000 IEEE	

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		Art Unit	2825 2827
		Examiner Name	
Sheet 2 of 3	Attorney Docket Number	CRF D-2768D/Kan	

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DL	10	"Single-Electron Devices and Their Applications," K.K. Likharev; Proceedings of the IEEE, Vol. 87, No. 4, April 1999	
	11	"Non-Volatile Si Quantum Memory with Self-Aligned Doubly-Stacked Dots," R. Ohba, N. Sugiyama, K. Uchida, J. Koga, A. Toriumi; IEEE 2000	
	12	"Modification of Indium Tin Oxide for Improved Hole Injection in Organic Light Emitting Diodes," Y. Shen, D.B. Jacobs, G.G. Malliaras, G. Koley, M.G. Spencer, A. Ioannidis; Adv. Mater. 2001, No. 16, 8/16	
	13	"Room Temperature Operation of a Quantum-Dot Flash Memory," J.J. Welser, S. Tiwari, S. Rishton, K.Y. Lee, Y. Lee; IEEE Electron Device Letters, Vol. 18, No. 6, June 1997	
	14	"Silicon Nano-Crystals Based MOS Memory and Effects of Traps on Charge Storage Characteristics," Y. Shi, S.L. Bu, X.L. Yuan, Y.D. Zheng; K. Saito, H. Ishikuro, T. Hiramoto; IEEE 1998	
	15	"A High Capacitive-Coupling Ratio (HiCR) Cell for 3 V-Only 64 Mbit and Future Flash Memories," Y.S. Hisamune, K. Kanamori, T. Kubota, Y. Suzuki, M. Tsukiji, E. Hasegawa, A. Ishitani, T. Okazawa, IEEE 1993	
	16	"Volatile and Non-Volatile Memories in Silicon with Nano-Crystal Storage," S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan, D. Buchanan; 1995 IEEE	
	17	"Multilevel Flash cells and their Trade-offs," B. Eitan, R. Kazerounian, A. Roy; G. Crisenza, P. Cappelletti, A. Modelli; 1996 IEEE	
	18	"Modeling and Design Study of Nanocrystal Memory Devices," M. She, Y-C King, T-J King, C. Hu; Dept. of Elect. Eng. and Comp. Sciences, U. of C., Berkely, CA	
DL	19	"A Four-State EEPROM Using Floating-Gate Memory Cells," C. Bleiker, H. Melchior; IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 3, June 1987.	

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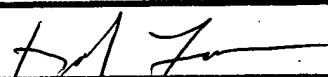
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		Art Unit	2018 2821
		Examiner Name	
Sheet 3 of 3	Attorney Docket Number	CRF D-2768D/Kan	

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DL	20	"A Multilevel Approach Toward Quadrupling the Density of Flash Memory," D.L. Kencke, R. Richart, S. Garg, S.K. Banerjee; IEEE Electron Device Letters, Vol. 19, No. 3, March 1998	
	21	"Data Retention of a SONOS Type-Two-Bit Storage Flash Memory Cell," W.J. Tsai, N.K. Zous, C.J. Liu, C.C. Liu, C.H. Chen, T. Wang, S. Pan, C-Y Lu; S.H. Gu; 2001 IEEE	
	22	"A Novel Approach to Controlled Programming of Tunnel-Based Floating-Gate MOSFET's," M. Lanzoni, L. Briozzo, B. Ricco; IEEE Jnl. of Solid-State Circuits, Vol. 29, No. 2, February 1994	
	23	"On the Universality of Inversion Layer Mobility in Si MOSFET's: Part I-Effects of Substrate Impurity Concentration," S-i Takagi, A. Toriumi, M. Iwase, H. Tango; IEEE Transactions on Electron Devices, Vol. 41, No. 12, December 1994	
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